Fraunhofer IPMS

Fraunhofer Institute for Photonic Microsystems IPMS

# CAN-CTRL – ISO CAN FD/CAN 2.0B/CAN XL CONTROLLER CORE

The CAN-CTRL IP core is a bus controller that carries out serial communication according to the CAN 2.0, CAN FD specification (ISO 11898-1: 2015 plus earlier ISO and Bosch specification) and CAN XL (CiA 610-1). It is compatible to ISO CAN FD and is certified as ISO 26262 ASIL-D ready.

The CAN protocol uses a multi-master bus configuration for the transfer of frames between nodes of the network and manages error handling with no burden on the host processor. The core enables users to set up economic and reliable links between various components. It appears as a memory-mapped I/O device to the host processor, which accesses the CAN-CTRL core to control the transmission and reception of frames. Optionally a stream interface can be used which allows to reduce the size of the memory inside the core.

The core is easy to integrate: it offers a simple generic processor interface and additional wrappers to allow the integration into AMBA AHB or APB bus systems. CAN-CTRL is flexible but still easy to use: it provides programmable interrupts, data and baud rates as well as a configurable number of independently programmable acceptance filters. It implements a flexible memory scheme, allowing fine-tuning of the core size to the require-ments of each specific application. The number of storable reception frames can be configured prior to synthesis. Two types of transmit buffers are implemented: a high-priority primary transmit buffer (PTB) and a lowerpriority secondary transmit buffer (STB). Optionally the core can be configured to include a stream based message interface. They can be included into or excluded from an implementation using configuration parameters.

The PTB can store one message, while the number of included buffer slots for the STB is synthesis-time configurable. The STB can operate in FIFO mode or in priority mode where automatically the message with the highest priority is transmitted first.

Moreover, an optional wrapper instantiating multiple CAN controller cores eases the integration in cases where multiple busnodes need to be controlled by the same host processor.

## CAN Specifications Support

- CAN 2.0 & CAN-FD (ISO 11898-1.2015, plus earlier ISO and Bosch specifications)
- CAN XL (CiA 610-1 specification)
- TTCAN (ISO 11898-4 level 1)
- Optimized for AUTOSAR and SAE J1939

## Applications

The CAN-CTRL core can be integrated in devices that use CAN or higher-layer CANbased communication protocols.In addition to traditional automotive applications, such devices are used in industrial (e.g. the CANopen and the DeviceNet protocols), aviation (e.g. the ARINC-825 and CANaerospace protocols), marine (e.g. the NMEA 2000 protocol) and other applications.

With its safety enhanced package it is also suitable for devices and systems in automotive, airborne, space, medical and other safety critical applications.


**Contact**

Monika Beck
+49 351 88 23-274
monika.beck@
ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Maria-Reiche-Strasse 2
01109 Dresden, Germany
www.ipms.fraunhofer.de


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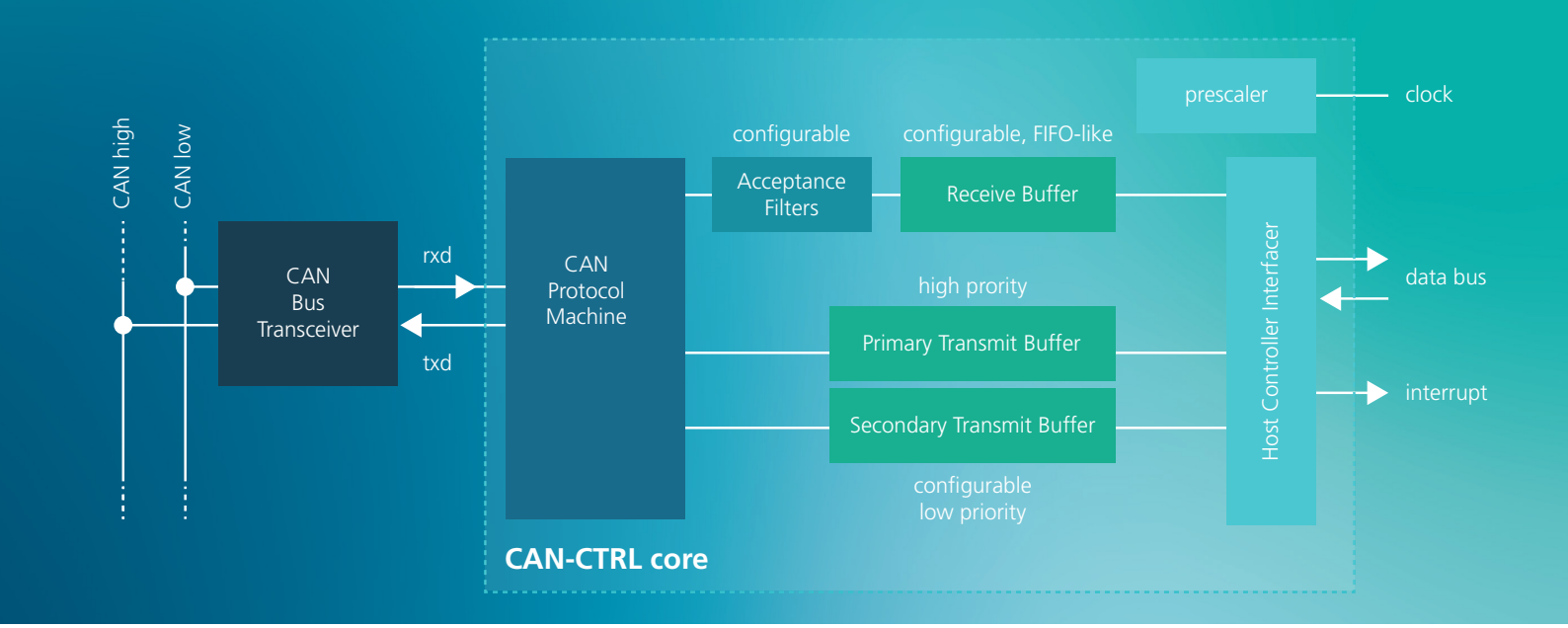


## Features

- Flexible CAN FD data rate, extended data field up to 64 bytes
- Error Analysis features enabling diagnostics, system maintenance and system optimization: last error type, arbitration lost position, error warning limit
- Listen-Only Mode enables CAN bus traffic analysis and automatic bit-rate detection
- Single Shot Transmission Mode
- 2 clock domains for CAN protocol machine and host controller interface enable usage of an optimal clock for CAN communication independent from the host clock (clock domain crossing)
- Time-triggered operation (TTCAN, ISO 11898-4)
- Supports ECC for SRAM & spatial redundancy for inner logic protection
- Time-stamping support, compliant to CiA's 603 specification
- Loop back mode for self-testing
- Optional stream interfaces for transmission and reception of frames

## Flexible Message Buffering and Filtering

- Configurable number of receive buffers
- One high-priority transmit buffer
- Configurable number of lower-priority transmit buffers
- 1 to 16 independently programmable 29-bit acceptance filters
- FIFO or priority mode for transmit buffers
- Optional memory protection using ECC

## Easy System Integration

- Platform independent implementation Xilinx, Intel, Microsemi, Lattice, Gowin FPGAs and any foundry technologies
- Programmable data rate up to 1 Mbit/s with CAN 2.0 and several Mbit/s with CAN FD or CAN XL option
- Programmable baud rate prescaler: 1 up to 1/256
- Flexible programmable interrupt sources
- Generic 32-bit host controller interface AHB and APB (32 bit), generic 8-bit and 16-bit optionally
- Memory can be implemented as Distributed-RAM or Block-RAM
- A single host can control multiple CAN bus nodes via an optional Multi-CAN wrapper
- Available in RTL, and portable to ASIC and FPGA technologies
- Compatible with CAN 2.0/FD/XL PHYs from NXP, MicroChip, OnSemi, Infineon, etc.

## Verification

The core has been tested by a Bosch reference model and is extensively proven in a large number of production designs.
It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

## Safety Enhanced Package

- SAM and FDMEA certified ISO-26262 ASIL D ready
- ISO-26262 documentation package.

## Deliverables

- VHDL or Verilog RTL source code
- Post-synthesis netlist for FPGA
- Testbenches (behavioral, post-synthesis verification)
- Simulation and synthesis scripts
- Safety enhanced version available ISO26262 ASIL-D Ready safety package
- Linux driver
- Documentation

## CANsec Controller IP Core

Fraunhofer IPMS offers a CANsec IP Core controller (CAN-SEC) an extension to the newly developed CAN XL protocol. It specifies a Layer 2 CAN security protocol that aims to protect the integrity and authenticity of the origin and confidentiality of data in CAN-based networks. It can be used with the CAN-XL IP Core (CAN-CTRL) of Fraunhofer IPMS, with any other CAN IP Core or in standalone operations.